Circuit simulation is an essential step within circuit design. Because of the increasing complexity of the Integrated Circuits, electronic companies need fast and accurate simulation software and there is a constant request at the companies to further improve the simulation software. Development of new, more advanced, transient simulation algorithms is an attractive way to increase the performance of this software. Mathematics is the basis to analyze the convergence properties.

The objective of this PhD research is to increase the performance of Pstar, the in-house analog circuit simulator at Philips and now of NXP Semiconductors, while properties like accuracy and robustness are maintained. In particular the convergence and stability properties of newly developed multirate time-integration algorithms is studied. Usually circuit models are large systems of differential-algebraic equations that are derived from Kirchhoff's conservation laws for currents and voltages and the constitutive relations for the electronic components. For a transient analysis one traditionally uses implicit time-integration schemes, like Backward Difference Formulae (BDF). All these schemes discretise the time on one time-grid. In contrast multirate algorithms use more than one time-grid and compute the slowly time-varying state elements only at coarsely distributed time-points, while the fastly time-varying state elements are computed at finer distributed timepoints. This makes a multirate algorithm potentially much faster for circuits with large low-frequency parts. There are many types of multirate time-integration methods that may differ in the order of the slow and fast integration and the treatment of the interface variables. We used a direct extension of the BDF scheme combined with Lagrange interpolation of the same order.

The standard theory for multistep methods does not hold anymore for multirate algorithms. Therefore we look at properties like stability and convergence in more detail. It turns out that the method is stable if the partitioned subsystems are individually stable and if the coupling is sufficiently weak. The discretisation error for a multirate method also contains an interpolation error due to the slow unknowns at the interface. This error component is not needed for ordinary multistep methods. It is possible to control this error by independent control of the coarse and fine macro and micro time-steps, respectively. The interpolation error and the coarse discretisation error is controlled by the macro stepsize, while the micro stepsize controls the fine discretisation errors for the fast state part. For multirate it is necessary to partitioning the system into a slow and a fast part. Therefore a part of the research is spent to the development and analysis of automatic partitioning algorithms. The underlying problem is a discrete optimisation problem, that can be handled by greedy-like methods. It is also possible to change the partitioning dynamically during the simulation, which is useful for moving active parts. All algorithms are implemented in Matlab; they work satisfactorily when tested for a variety of circuit models. Furthermore a
multirate implementation including error control and dynamical partitioning is created in the circuit simulator Pstar itself.

Besides multirate time-integration also model order reduction is studied, which transforms the large data models into smaller and simpler models, that still give the proper accuracy, but that are much cheaper to solve. Because IC models are nonlinear, nonlinear reduction techniques are considered in particular, like POD. In particular we focused on the problem to reduce the evaluation costs of these reduced models.

A proper use of multirate and model order reduction is able to speed up transient simulation in general and is significantly faster (more than an order) for redundant circuit models, while the accuracy and robustness are maintained. Redundancy occurs if the state elements have many correlations, or if the sampled state signal has correlations in time.